**GI/ITG/GMA Technical Committee "Dependability and Fault Tolerance" (VERFE)** and
**DFG Priority Program SPP 1500 "Dependable Embedded Systems"**

# 13th Workshop on Dependability and Fault Tolerance (VERFE'17)

in conjunction with **30th ARCS 2017,** Vienna, Austria, April 3th – 6th, 2017

# Call for Papers

## Background and Focus

Although the basic reliability of hardware and software components has improved over decades, their increasing number causes severe problems. Moreover, in recent years it can be observed that in an increasing number of devices, e.g. cars, digital components are integrated into environments of other physical components. Here, the complexity and number of interactions with these components creates problems with regard to maintaining a dependable operation of the entire system in case of faults or external disturbances.

While this is not a problem with microprocessors there, shrinking feature sizes, higher complexity, lower voltages, and higher clock frequencies increase the probability of design-, manufacturing-, and operational faults, making fault tolerance techniques in general purpose processors to be of crucial importance in the future. As simple solutions (such as TMR) easily can get too expensive, the ability to trade increased reliability against performance/power overhead will become important, resulting in light-weight fault tolerance techniques implemented in hardware, but controllable from higher software layers.

This workshop aims at presenting contributions and work-in-progress from the research area of dependable and fault tolerant computing in order to bring together scientists working in related fields.

## Topics

Contributions on the topic of "Dependable Embedded Systems" are of particular interest; contributions on general topics of dependability and fault tolerance are also welcome but not limited to:

- reliability models for hardware and software
- modeling and simulation of fault-tolerant systems
- fault-tolerant systems and system components
- formal verification of systems
- testing of hardware and software
- fault treatment
- detection and correction of transient faults
- quantitative assessment of reliability improvements
- safety-critical applications
- timeliness problems
- dependability of networks
- dependability of embedded systems
- highly available systems
- dependable organic computing
- self-organization within redundant systems
- dependable ubiquitous and pervasive computing
- composability of dependable systems
- dependable mechatronic systems / micro systems
- dependability of mobile and wireless systems
- robustness and robustness metrics
- validation and verification
- fault models and fault model abstraction
- fault-injection techniques
- software-controlled fault tolerance
- on-chip backward recovery techniques (e.g. pipeline flush and re-execution)
- forward recovery techniques (notification of higher layers)
- fault-tolerant caches
- dynamic re-use of currently unused resources in processors for fault-tolerance

## Information for Authors

**Accepted papers will be published by VDE and IEEExplore.**
**Selected papers will appear in the FERS Journal (0724-5319).**
The workshop will focus on research presentations as well as brainstorming sessions.
Therefore, two kinds of contributions are welcome:

- research papers documenting results of scientific investigations and
- position papers proposing strategies or discussing open problems.

## Deadlines:

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| Submission: | *** **EXTENDED January 31, 2017** (extended abstracts (3-4 pages) or full papers, PDF) *** to: bernhard.fechner@fernuni-hagen.de |
| Notification: | **February 13, 2017** |
| Camera-ready: | **February 20, 2017** (max. 13 pages); will appear in ARCS 2017 Workshop Proceedings. |

VERFE'17 Workshop site: http://arcs2017.itec.kit.edu/VERFE.pdf
Further information about ARCS 2017: http://arcs2017.itec.kit.edu/

## Workshop Chairs

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